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Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>03 August 2001</u>.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-37</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-3,8-13,16-20,23,26-30 and 35-37</u> is/are rejected.

7)☒ Claim(s) <u>4-7,14,15,21,22,24,25 and 31-34</u> is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☒ All b)☐ Some * c)☐ None of:

      1.☒ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

1.   DETAILED ACTION

2.   *Claim Objections*

3.   Claim 20 is objected to because of the following informalities:

4.   Claim 20 is not grammatically correct.

5.   Appropriate correction is required.

6.   *Claim Rejections - 35 USC § 112*

7.   The following is a quotation of the second paragraph of 35 U.S.C. 112:

8.   The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9.   Claim 27 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for

failing to particularly point out and distinctly claim the subject matter which applicant regards as

the invention.

10.   Claim 27 recites the limitation "the signals". There is insufficient antecedent basis for

this limitation in the claim since there are many signals.

11.   Claim 27 recites the limitation "the multiplication resulting values". There is insufficient

antecedent basis for this limitation in the claim.

12.   *Claim Rejections - 35 USC § 103*

13.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

14.   A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15.   Claims 1-3, 8-13, 16-20, 23, 26, 28-30, 35-37 are rejected under 35 U.S.C. 103(a) as

being unpatentable over Wright 6,798,843. Here is how the reference teaches the claims:

16.   As per claim 1: A predistortion digital linearizer, comprising a predistorter (Wright fig. 1:

52) coupled to receive an input signal (Wright fig. 1: Vm(t)) and a control signal (Wright fig. 1:

x+(t)) to generate a predistorted signal (Wright fig. 1: output of 52 Vd(t)); an up-converter

coupled to receive the predistorted signal and convert it into a radio frequency signal (Wright fig.

1: 58), a high power amplifier (HPA) to receive and amplify the radio frequency signal outputted

from the up-converter (Wright fig. 1: 60); a feedback unit coupled to receive an output of the

HPA and down-convert the received signal into a baseband signal (Wright fig. 1: 66), and an

adaptation processing unit coupled to receive the baseband signal and a delayed digital input

signal to generate the control signal (Wright fig. 1: 70; paragraph 34 col. 9 lines 27-34: "The

ACPCE 70 preferably computes compensation parameters in an off-line mode using previously-

captured samples).

17.   What Wright does not teach is that 70 is receiving a delayed signal since it is shown as

receiving a digital input signal Vm(t). It is common knowledge that adding a delay device

delays a signal. It would have been obvious, to one of ordinary skill in the art, at time the

invention was made, to modify the prior art teaching of Wright with a delayed signal as recited

by the instant claims. One would be motivated to do so because Wright suggests that it wants to

eliminate the difference between the input and the amplifier output (Wright col. 8 lines 34-43:

"The Adaptive Control Processing and Compensation Estimator (ACPCE) 70 computes and

eliminates the time delay difference between digital samples of the observed amplifier output

and the ideal input signal.") where the amplifier output is delayed since that signal has to go

through multiple components; thus adding a delay to the input would accomplish this goal.

18.   As per claim 2: The device of claim 1, wherein the predistorter comprises a power

measuring unit to measure a power magnitude of the input signal (Wright fig. 3: 52F, 52G); a

work function generator (Wright fig. 3: 52H) configured to receive an amount of the power

measuring unit (Wright fig. 3: 52H) and the control signal (Wright fig. 3: X+) and configured to

generate a predistortion work function for determining a distortion size of the input signal

according to the magnitude of the input signal (Wright fig. 3: 52I); and a complex coupler

(Wright fig. 3: 52B) configured to receive and complex-couple the predistortion work function

(Wright fig. 3: 52I) and the input signal (Wright fig. 3: Vm(t) via 52A) to generate the

predistorted signal (Wright fig. 3: 52B).

19.   As per claim 3. The device of claim 2, wherein the power measuring unit comprises a

first square unit to square a first phase digital input signal and output a first square value (Wright

fig. 37: inside the magnitude unit would be the I^2 shown in $p=f(I^2+Q^2)$); a second square

unit to square a second phase digital input signal and output a second square value (Wright fig.

37: inside the magnitude unit would be the Q^2 shown in $p=f(I^2+Q^2)$); and an adder

configured to add the first and second square values to obtain a magnitude of the input signal

(Wright fig. 37: inside the magnitude unit would be the addition of I^2 and Q^2 shown in

$p=f(I^2+Q^2)$).

20.   As per claim 8: The device of claim 1, wherein the input signal is a digital input signal

and the predistorted signal is a predistorted digital signal, and wherein the up-converter

comprises first and second digital-to-analog converters to convert the predistorted digital signal

to an analog signal (Wright fig. 31a: 2 DACs 54); and a modulator to modulate the analog signal

outputted from the digital-to-analog converters (Wright fig. 31A: 58).

21.   As per claim 9. The device of claim 1, wherein the feedback unit comprises a

demodulator to demodulate the output of the HPA (Wright fig. 31A: 66); and first and second

analog-to-digital converters to convert the demodulated analog signal outputted from the

demodulator to a digital signal (Wright fig. 31A: 68). Wright does not teach two ADC's as it

only teaches one ADC; however, it would have been obvious, to one of ordinary skill in the art,

at time the invention was made, to modify the prior art teaching of Wright with two ADCs as

recited by the instant claims, because Wright suggests two ADCs in fig. 31B and having two

ADC's here would accomplish having parallel processing to increase processor speed. Also, as

Wright teaches two DACs out of 52, and ADC is the opposite of DAC, it is obvious to duplicate

parts of an invention since doing so requires routine skill in the art.

22.   As per claim 10: The device of claim 1 wherein the adaptation processing unit comprises

a delay unit to delay the input signal for a prescribed period of time (Wright paragraph 34: "The

ACPCE 70 preferably computes compensation parameters in an off-line mode using previously-

captured samples); and a digital signal processor coupled to receive the delayed input signal and

the baseband signal from the feedback unit to generate the control signal. (Wright paragraph 34:

"The ACPCE 70 preferably computes compensation parameters in an off-line mode using

previously-captured samples of the amplifier's input and output signals.")

23.   As per claim 11. The device of claim 1, further comprising a gain control circuit to

receive the input signal and control a gain of the input signal according to a gain control signal,

and output a gain controlled input signal to the predistorter (Wright fig. 12: Gain controlled based on Pin; fig. 51: 130).

24.   As per claim 12. The device of claim 11, wherein a gain of the gain control signal (Wright fig. 51: 130) is set according to a gain of the delayed input signal (Wright paragraph 34: "The ACPCE 70 preferably computes compensation parameters in an off-line mode using previously-captured samples; arrow from 130 to 70), an output level of the HPA estimated by using the feedback digital output signal (Wright fig. 51: bottom input into 130), and a desired HPA output level (Wright fig. 12).

25.   As per claim 13: The device of claim 11, wherein the gain control signal can be provided by the adaptation processing unit (Wright fig. 51: 130 and 70 are joined) and can be provided by an external source (Wright fig. 51: the source of the Vm(t) signal provides the gain of that signal).

26.   As per claim 16: The device of claim 1, wherein the predistorted digital signal has a distortion characteristic that is opposite of a distortion characteristic of the HPA. such that an output of the HPA is substantially non-distorted (Wright: this is the purpose of predistortion).

27.   As per claim 17: The device of claim 1, wherein each of the input signal, the predistorted signal, and the baseband signal is a digital signal (Wright fig. 2: left side of dotted line is in the digital domain).

28.   As per claim 18: A predistortion digital linearizer, comprising a digital predistorter (Wright fig. 1: 52) to distort a digital (Wright fig. 1: digital domain) input signal (Wright fig. 1: Vm(t)) according to a control signal (Wright fig. 1: x+(t)); a digital-to-analog converter coupled to convert an output signal of the digital predistorter to an analog signal (Wright fig. 1: 54); a

modulator coupled to modulate an output signal of the digital-to-analog converter to a frequency

of a carrier (Wright fig 1: 58); a high power amplifier (HPA) coupled to power-amplifier an

output signal of the modulator (Wright fig. 1: 60); a demodulator coupled to receive an output

signal of the HPA and demodulate it to a baseband signal (Wright fig. 1: 66); an analog-to-digital

converter coupled to convert the analog baseband signal outputted from the demodulator to a

digital signal (Wright fig. 1: 68); and a digital signal processor coupled to compare an output

signal of the analog-to-digital converter to the digital input signal and generate the control signal

to control a distortion degree of the digital predistorter (Wright fig. 1: 70).

29.   What Wright does not teach is that a modulating to a frequency of a carrier. It is

common knowledge that when a signal is around a carrier frequency, it is also on the carrier

frequency. It would have been obvious, to one of ordinary skill in the art, at time the invention

was made, to modify the prior art teaching of Wright with modulating to a frequency of a carrier

as recited by the instant claims, because Wright suggests in col. 1 lines 18 to 27 that a

transmitted signal is concentrated around a carrier frequency. Since it is around the carrier

frequency, it is also on the carrier frequency.

30.   ´ As per claim 19. The device of claim 18a wherein the predistorted digital signal has a

distortion characteristic that is opposite of a distortion characteristic of the HPA , such that an

output of the HPA is substantially non-distorted. (Wright: this is the purpose of predistortion)

31.   As per claim 20. The device of claim 1 8: further comprising a coupler to receive and split

off a portion of the output signal the HPA to provide to the demodulator (Wright fig. 1: 62).

32.   As per claim 23: A predistortion digital linearizer, comprising a gain control circuit to

receive and control a level of a digital input signal according to a gain control signal; predistorter

coupled to predistort the gain controlled digital input signal in accordance with a control signal; a

digital-analog converter coupled to convert the predistorted digital signal to an analog signal; a

modulator coupled to modulate the analog signal outputted from the digital-analog converter; a

high power amplifier (HPA) coupled to power-amplifier an output 01* the modulator, a

demodulator coupled to demodulate the amplified signal outputted from the HPA; an analog-

digital converter coupled to convert an analog baseband signal outputted from the demodulator

to a digital signal; (up to here discussed above) a delay circuit coupled to delay the digital input

signal for a prescribed period of time (Wright paragraph 34, col. 9 lines 27-34: "The ACPCE 70

preferably computes compensation parameters in an off-line mode using previously-captured

samples); and a digital signal processor coupled to receive the output signal of the analog-digital

converter and an output of the delay circuit to generate the gain control signal (Wright fig. 12:

Gain controlled based on Pin) and the control signal (Wright fig. 1: x+(t)).

33.   What Wright does not teach is that 70 is receiving a delayed signal since it is shown as

receiving a digital input signal Vm(t). It is common knowledge that adding a delay device

delays a signal. It would have been obvious, to one of ordinary skill in the art, at time the

invention was made, to modify the prior art teaching of Wright with a delayed signal as recited

by the instant claims. One would be motivated to do so because Wright suggests that it wants to

eliminate the difference between the input and the amplifier output (Wright col. 8 lines 34-43:

"The Adaptive Control Processing and Compensation Estimator (ACPCE) 70 computes and

eliminates the time delay difference between digital samples of the observed amplifier output

and the ideal input signal.") where the amplifier output is delayed since that signal has to go

through multiple components; thus adding a delay to the input would accomplish this goal.

34.   As per claim 26: The device of claim 23, wherein the digital signal processor is

configured to adaptively control a gain (Wright fig. 51: 130) and predistortion (Wright fig. 51:

52) of the digital input signal (Wright fig. 51: Vm(t)) according to an output level of the HPA

(Wright fig. 51: output of 60 eventually into 130), a delayed digital input signal (Wright

paragraph 34: "The ACPCE 70 preferably computes compensation parameters in an off-line

mode using previously-captured samples), and a desired output level (Wright fig. 12).

35.   As per claim 28. A predistortion linearizer, comprising a digital predistorter coupled to

receive first and second digital input signals (Wright fig. 1: 52 receives first and second signals

at different times) and a digital control signal to generate first and second digital conditioned

signals having a prescribed distortion characteristic (Wright fig. 1: output of 70); an amplifier

circuit coupled to receive the first and second digital conditioned signals, convert the digital

signals to analog signals (Wright fig. 1: 54), modulate the analog signals (Wright fig. 1L 58), and

amplify the modulated signal (Wright fig. 1: 60); and a feedback circuit coupled to receive a

portion of the amplified signal and delayed first and second digital input signals to generate the

digital control signal (Wright fig. 1: 66, 68, 70), wherein the prescribed distortion characteristic

is an inverse of a distortion characteristic of the amplifier circuit (Wright col. 8 lines 3-21).

36.   What Wright does not teach is delayed signals. It is common knowledge that adding a

delay device delays a signal. It would have been obvious, to one of ordinary skill in the art, at

time the invention was made, to modify the prior art teaching of Wright with a delayed signal as

recited by the instant claims. One would be motivated to do so because Wright suggests that it

wants to eliminate the difference between the input and the amplifier output (Wright col. 8 lines

34-43: "The Adaptive Control Processing and Compensation Estimator (ACPCE) 70 computes

and eliminates the time <u>delay</u> difference between digital samples of the observed amplifier

output and the ideal input signal.") where the amplifier output is delayed since that signal has to

go through multiple components; thus adding delays to the inputs would accomplish this goal.

37.   Claims 29, 30, 35-37 are discussed above with respect to other claims.

38.   Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wright 6,798,843

in view of Lynch 4,875,045. Here is how the reference teaches the claims:

39.   As per claim 27: A method for controlling a gain of a predistortion digital linearizers

comprising: determining an output level of a high power amplifier using a feedback digital

output signal (Wright fig. 51: output of 66 and 68 due to feedback); computing a gain control

signal for gain control (Wright fig. 51: 130) by using the determined output level (Wright fig. 51

bottom input into 130), a desired output level (Wright fig. 12), and a level of a digital input

signal delayed for a prescribed period of time (Wright paragraph 34: "The ACPCE 70 preferably

computes compensation parameters in an off-line mode using previously-captured samples);

multiplying the current digital input signal by the gain control signal to control the level of the

digital input signal (Wright fig. 51: 132); and maintaining a sign bit (Lynch 4,875,045 fig. 3: 25a

sign bit feedback) of the multiplication resulting value, taking the remaining lower bits as a

predetermined number of bits, and adjusting the digits of the signals before and after

multiplication (rejected under 112) (Wright fig. 51: 130 gain control is adjusted before and after

multiplication).

40.   What Wright does not teach is maintaining a sign bit. What Lynch teaches is maintaining

a sign bit. Thus, it would have been obvious, to one of ordinary skill in the art, at time the

invention was made, to arrive at maintaining a sign bit as recited by the instant claims, because

the combined teaching of Wright with Lynch suggest multiplication while maintaining a sign bit

as recited by the instant claims. Furthermore, one of ordinary skill in the art, would have been

motivated to combine the teachings of Wright with Lynch because Wright suggests

multiplication (something broad) in general and Lynch suggests the beneficial use of maintaining

a sign bit, such as to not introduce significant noise and distortion (Lynch col. 1 line 63), in the

analogous art of variable gain.

41.   *Allowable Subject Matter*

42.   Claims 4-7, 14-15, 21-22, 24-25, 31-34 are objected to as being dependent upon a

rejected base claim, but would be allowable if rewritten in independent form including all of the

limitations of the base claim and any intervening claims.

43.   Conclusion

44.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Pankaj Kumar whose telephone number is (571) 272-3011. The

examiner can normally be reached on Mon, Tues, Thurs and Fri after 8AM to after 6:30PM.

45.   If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Mohammad H. Ghayour can be reached on (571) 272-3021. The fax phone number

for the organization where this application or proceeding is assigned is 703-872-9306.

46.   Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

47.   48.

49.   PK

MOHAMMED GHAYOUR
SUPERVISORY PATENT EXAMINER